REMARKS

These remarks are in response to the Office Action dated May 5, 2006 (Office Action). As this reply is timely filed, no fee is believed due. Claims 1, 8, and 15, the abstract, and paragraph 7 have been amended to clarify various aspects of the present invention. Support for these amendments can be found throughout the Applicant's specification and, more particularly, at paragraphs [0016], [0031], and [0033]-[0036]. No new matter has been introduced.

In the Office Action, the abstract of the disclosure has been objected to because "it is not clear what Applicant intended to mean by [the] phrase 'A final delay for connections of the circuit design can be predicted were connection overlaps to be removed.'" The quoted passage has been amended to read "A final delay for connections of the circuit design can be predicted with connection sharing removed." Accordingly, withdrawal of the objection to the abstract is respectfully requested.

Claims 1, 8, and 15 have been objected to because of informalities relating to the usage of the word "were" within each claim. Claims 1, 8, and 15 have been amended to recite "predicting a final delay for the connections of the circuit design with connection sharing removed". The word "were" has been replaced with the word "with". The phrase "has been" has been deleted. Those skilled in the art will appreciate that the amendments to Claims 1, 8, and 15 have been made only to correct minor informalities. As such, withdrawal of the objection to claims 1, 8, and 15 is respectfully requested.

Claims 1-21 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The Office Action asserts that a step/relationship is missing between the second and third limitations of claims 1, 8, and 15, such as under what condition and when connection sharing has been removed and how the second and third limitations are related to the preamble.

Applicant respectfully disagrees with this contention. MPEP § 2172.01 states, in relevant part, that a claim does not necessarily fail to comply with 35 U.S.C. § 112, second paragraph, where the various elements "are not directly functionally related,

[or] do not directly intercooperate." In claims 1, 8, and 15, the identification of connections of the circuit design that do not conform to timing constraints relies upon both the initial delays and the final delays, thereby establishing a relation between the second and third steps. Further, connection sharing is an attribute that is indicative of congestion, which relates to the preamble. As such, Applicant believes that claims 1, 8, and 15 do conform to the requirements of 35 U.S.C. § 112, second paragraph.

Notwithstanding, the limitation relating to "routing connections" within each of claims 1, 8, and 15 has been amended to further recite "wherein the routed circuit design includes at least one instance of connection sharing". As noted, connection sharing is indicative of congestion. Also, the limitation relating to "predicting a final delay" has been amended to further recite "wherein the final delays are predicted according to initial delays and a measure of connection sharing within the circuit design". In addition to the relations discussed above, an additional relation between the second and third steps exists in that the final delays are predicted according, at least in part, to the initial delays. With regard to the preamble, the final delays are predicted, at least in part, according to a measure of connection sharing. In light of the foregoing, withdrawal of the 35 U.S.C. § 112, second paragraph, rejection of claims 1-21 is respectfully requested.

Turning to the rejections on the art, claims 1, 5-8, 12-15, and 19-21 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication 2004/0243953 to Ramachandran et al. (Ramachandran). Ramachandran discloses methods and apparatuses for automatically modifying a circuit design according to the sensitivity of the circuit design to one or more design parameters. Ramachandran, however, does not teach or suggest the Applicant's invention as recited in the claims. In particular, Ramachandran does not teach or suggest the use of two different delay calculations, where one is dependent upon connection sharing, to identify connections of the circuit design in need of further optimization or processing.

Regarding claims 1, 8, and 15, the Office Action contends that Ramachandran teaches each feature recited by these claims. In particular, it is asserted that "routing connections of a circuit design for the integrated circuit in a delay mode, wherein the

routed circuit design includes at least one instance of connection sharing" is taught by Ramachandran. In support, paragraphs 28, 42, and 70 of the Ramachandran specification have been cited.

Applicant's claims explicitly recite that a delay mode is used to route connections of a circuit design, and that. the routing of the circuit design produces at least one instance of connection sharing. In contrast, paragraphs 28, 42, and 70 of Ramachandran do not teach or suggest that a circuit design is routed using a delay mode that results in at least one instance of connection sharing.

Paragraph 32 of Ramachandran has been cited as teaching "calculating an initial delay for the connections of the circuit design" as recited by claims 1, 8, and 15. Since claims 1, 8, and 15 recite that the circuit design is routed in a manner that includes at least one instance of connection sharing, the initial delays are determined with the shared connections in place. In paragraph 32, Ramachandran describes the estimation of the sensitivity of a circuit design to various timing parameters as well as using transformations in and near critical portions of the circuit design to reduce variation in the delay on critical paths. While Ramachandran mentions critical paths, paragraph 32 does not teach or suggest the calculation of initial delays for a circuit design that includes connection sharing.

Paragraph 42 of Ramachandran has been cited for teaching "predicting a final delay for the connections of the circuit design with connection sharing removed, wherein the final delays are predicted according to the initial delays and connection sharing within the circuit design". In paragraph 42, Ramachandran states:

> For example, when detailed placement is performed during physical synthesis, the legal locations of all instances in the design are available. A quick global route estimation can be performed to determine the most likely route that a net would assume. From these estimated routes, a predicted congestion map of the routes is determined.

Paragraph 42 includes no discussion of a predicted final delay for connections. As noted, Ramachandran does not mention the determination of an initial delay based upon a routing of the circuit design that includes connection sharing. Ramachandran further lacks any discussion relating to the use of a final delay that is predicted based in part upon a measure of connection sharing within the circuit design. Indeed,

Ramachandran includes no teaching or suggestion that the estimation of any delay parameter is dependent upon connection sharing within the circuit design. Claims 1, 8, and 15 recite that the final delays are predicted according to the initial delays and a measure of connection sharing within the circuit design.

Paragraphs 44, 46, and 51 of Ramachandran have been cited for teaching "identifying connections of the circuit design that do not conform with timing constraints based upon at least one of the initial delays or the final delays". Paragraph 44 discloses that layer assignments of nets can influence capacitance and resistance of wires, which can change timing. Paragraph 46 discloses that increases in wire length can be estimated using a function that is dependent upon route congestion. Paragraph 51 discloses that a timing objective parameter typically is a function of capacitance.

Applicant reiterates that Ramachandran does not teach or suggest the use of initial delays and final delays in identifying connections that do not conform to timing constraints. As noted, the initial delay is determined by routing the circuit design in delay mode where the resulting circuit design includes one or more instances of connection sharing. The final delay is predicted according to the initial delay and a measure of connection sharing within the circuit design. None of the paragraphs cited above teaches or suggests the use of multiple delay measurements or calculations. Further, none of the paragraphs cited above teaches or suggests that such delays reflect the presence or absence of connection sharing within the circuit design.

In sum, Ramachandran fails to teach or suggest the features of the Applicant's invention as recited in claims 1, 8, and 15. Claims 5-7, 12-14, and 19-21 are believed to be allowable by virtue of their dependence upon claims 1, 8, and 15 respectively. Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejection with respect to claims 1, 5-8, 12-15, and 19-21 is respectfully requested.

Claims 2-4, 9-11, and 16-18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Ramachandran as applied to claims 1, 8, and 15 above, and further, in view of U.S. Patent Application Publication 2004/0040007 to Harn (Harn). The Office Action contends that Ramachandran teaches the limitations of independent claims 1, 8, and 15, but does concede that Ramachandran "lacks the specifics

regarding predicting the final delay for the connections." It is asserted, however, that Harn teaches such detail.

Harn, however, fails to cure the deficiencies of Ramachandran. Paragraphs 70 and 71 have been cited in support of the rejection of claims 2-4, 9-11, and 16-18. In paragraphs 70 and 71, Harn states:

> [0070] When more than one block 128 is identified at step 94 as having capacity to receive the cell to be relocated, the P&R tool selects the least congested block 128 having such spare capacity. To do so the P&R tool (step 134) first computes an overflow factor $F_{i,j}$ for each block $B_{i,j}$ having spare capacity as follows:
>
> $$F_{i,j} = D_{i,j} - S_{i,j}$$
>
> [0071] where $B_{i,j}$ is the block at the intersection of the i^{th} row and j^{th} column of the array, $S_{i,j}$ is the total available area within block $B_{i,j}$ for routing nets and demand $D_{i,j}$ the total amount of area demanded by the nets within the block. Nets are routed on various conductive layers formed above the surface of an IC's semiconductor substrate, so the routing resource supply S of each block is the total area of the routing layers within that block. The P&R tool computes the routing resource demand $D_{i,j}$ for each block as the sum of areas occupied by nets routed through the block in the trial routing plan. Where two conflicting nets overlap, the area in which the overlap is counted twice when computing demand $D_{i,j}$. The routing factor for a block 128 is positive when it is so congested that the demand for routing resources exceeds the supply. A block 128 having sufficient spare capacity to receive the cell and otherwise having the smallest (most negative) overflow factor $F_{i,j}$ is then selected to receive the cell (step 136).

As illustrated by the above passage, the overflow parameter of Harn is used in determining whether a given block in a circuit design has sufficient capacity to receive a cell that is being relocated. The overflow parameter is used to relocate cells and not to determine whether a given connection meets a timing requirement. Thus, the overflow parameter of Harn and the final delay of the Applicant's invention convey different information and are used for different purposes.

Further distinguishing Harn from Applicant's invention, the prediction of a final delay as taught by Applicant depends upon the "number of connections sharing each wire by said routing step. Applicant's claims are clear in that the predicted final delay

depends upon connection sharing and that connection sharing is determined on a per wire basis. By comparison, Harn is clear that area measurements are used in calculating the overflow parameter. Harn does not teach or suggest evaluating connection sharing on a per wire basis.

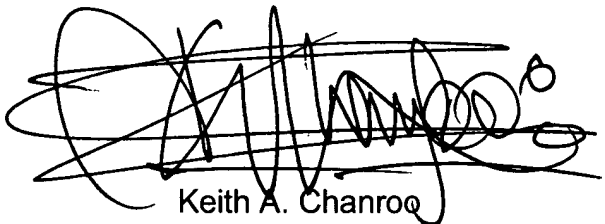
In view of the foregoing, Harn fails to teach or suggest the detail that is lacking in Ramachandran. As neither Ramachandran, Harn, nor any combination thereof teaches or suggests the Applicant's invention as claimed, withdrawal of the 35 U.S.C. § 103(a) rejection of claims 2-4, 9-11, and 16-18 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-7710 (Pacific Standard Time).

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 1, 2006.

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Signature